In the Claims

1-6. (Cancelled)

7. (Withdrawn) A semiconductor device having multi-layered interconnection lines comprising:

a plurality of lower interconnection lines formed to be parallel in a single direction on a semiconductor substrate, the lower interconnection lines each having an end aligned with each other on a straight line;

an interlayer insulating layer covering an entire surface of the substrate having the lower interconnection lines; and

a plurality of upper interconnection lines formed to overlap with the lower interconnection lines on the interlayer insulating layer.

8. (Withdrawn) The semiconductor device of claim 7, wherein the upper interconnection lines extend past the ends of the lower interconnection lines.

9. (Withdrawn) The semiconductor device of claim 7, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

10. (Withdrawn) The semiconductor device of claim 7, wherein the interlayer insulting layer is formed with at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

11. (Withdrawn) The semiconductor device of claim 7, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

12. (Currently Amended) A semiconductor device having multi-layered interconnection lines, the semiconductor device comprising:

~~parallel~~ lower interconnection lines ~~formed~~ disposed on a semiconductor substrate, the lower interconnection lines substantially coplanar, the lower interconnection lines aligned in a first direction and disposed parallel to one another, the lower interconnection lines

including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, an end of the first lower interconnection line and an end of the second lower interconnection ~~lines extending~~ line disposed a substantially equal distance ~~past~~ away from an end of the third lower interconnection line;

an interlayer insulating layer ~~formed~~ disposed on ~~an entire~~ a surface of the substrate having the lower interconnection lines; and

upper interconnection lines disposed on the insulating layer, the upper interconnection lines substantially coplanar, the upper interconnection lines aligned in the first direction and and disposed parallel to each other, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection ~~line formed on the insulating layer, the first, second, and third upper interconnection lines overlapping the first, second, and third lower interconnection lines, respectively~~

13. (Original) The semiconductor device of claim 12, further comprising:

a fourth upper interconnection line formed on the insulating layer and located on the same line as the third upper interconnection line but separated from it by a distance, the distance between the third and fourth upper interconnection lines being greater than a longest focus distance.

14. (Original) The semiconductor device of claim 12, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

15. (Previously presented) The semiconductor device of claim 12, wherein the interlayer insulating layer comprises at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

16. (Original) The semiconductor device of claim 12, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

17. (Withdrawn) A semiconductor device having multi-layered interconnection lines, the semiconductor device comprising:

a plurality of parallel lower interconnection lines formed on a semiconductor substrate, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower interconnection line;

an interlayer insulating layer formed on an entire surface of the substrate having the lower interconnection lines; and

a first upper interconnection line and a second upper interconnection line formed on the insulating layer, the first and second upper interconnection lines overlapping the first and second lower interconnection lines, respectively.

18. (Withdrawn) The semiconductor device of claim 17, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

19. (Withdrawn) The semiconductor device of claim 17, wherein the interlayer insulting layer comprises at least one layer selected from a group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

20. (Withdrawn) The semiconductor device of claim 17, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

21-22. (Cancelled)

23. (Currently Amended) A semiconductor device comprising:

lower interconnection lines, the lower interconnection lines substantially coplanar and disposed parallel to each other on a semiconductor substrate, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower interconnection line;

an interlayer insulating layer disposed on a surface of the substrate having the lower interconnection lines; and

upper interconnection lines, the upper interconnection lines substantially coplanar and disposed parallel to each other on the insulating layer, the upper interconnection lines disposed parallel to and aligned in the same direction as the lower interconnection lines, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line between the first and second upper interconnection lines.

24. (Withdrawn) The semiconductor device of claim 23, the upper interconnection lines further comprising a fourth upper interconnection line disposed parallel to the first and the second upper interconnection lines, the fourth upper interconnection line further disposed such that a vertical plane running along the length of the third upper interconnection line and the fourth upper interconnection line bisects the third upper interconnection line and the fourth upper interconnection line, an end of the third upper interconnection line and an end of the fourth upper interconnection line separated from each other by a distance that is greater than a longest focus distance.

25. (Previously presented) The semiconductor device of claim 23, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

26. (Previously presented) The semiconductor device of claim 23, wherein the interlayer insulating layer comprises at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

27. (Previously presented) The semiconductor device of claim 23, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

28. (Withdrawn) A semiconductor device comprising:

lower interconnection lines disposed parallel to each other on a semiconductor substrate, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower interconnection line;

an interlayer insulating layer disposed on a surface of the substrate having the lower interconnection lines; and

upper interconnection lines disposed parallel to each other on the insulating layer, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line between the first and second upper interconnection lines, the first, second, and third upper interconnection lines aligned with the first, second, and third lower interconnection lines such that a first vertical plane running along the length of the first lower interconnection line and the first upper interconnection line bisects the first lower interconnection line and the first upper interconnection line, a second vertical plane running along the length of the second lower interconnection line and the second upper interconnection line bisects the second lower interconnection line and the second upper interconnection line, and a third vertical plane running along the length of the third lower interconnection line and the third upper interconnection line bisects the third lower interconnection line and the third upper interconnection line.

29. (Withdrawn) The semiconductor device of claim 28, the upper interconnection lines further comprising a fourth upper interconnection line that is also bisected in a lengthwise direction by the third vertical plane, an end of the fourth upper interconnection line and an end of the third upper interconnection line separated from each other by a distance that is greater than a longest focus distance.

30. (Withdrawn) The semiconductor device of claim 28, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

31. (Withdrawn) The semiconductor device of claim 28, wherein the interlayer insulating layer comprises at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

32. (Withdrawn) The semiconductor device of claim 28, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

33. (New) The semiconductor device of claim 12, wherein the upper interconnection lines and the lower interconnection lines are disposed such that a vertical projection of each of the first upper interconnection line, second upper interconnection line, and third interconnection line on upper surfaces of the first lower interconnection line, second lower interconnection line, and third lower interconnection line, respectively, lies within the boundaries defined by the upper surfaces of the first lower interconnection line, the second lower interconnection line, and the third lower interconnection line, respectively.

34. (New) The semiconductor device of claim 23, wherein the lengths of the upper interconnection lines and the lengths of the lower interconnection lines are aligned in the same direction.